AMENDMENT

Please amend the application as follows:

In the Claims:

Please cancel claims 3, 19, and 30 (claim 2 canceled previously). Please amend claims 1, 4, 18, 20, 29, and 31. The current version of all the claims follows:

1. (Currently amended) A radio-frequency (RF) receiver circuitry, comprising:

down-converter circuitry configured to accept a received radio-frequency signal, the down-converter circuitry further configured to process the received radio-frequency signal to provide an in-phase down-converted signal and a quadrature down-converted signal;

analog-to-digital converter (ADC) circuitry configured to receive the in-phase and quadrature down-converted signals and to provide an in-phase digital output signal and a quadrature digital output signal;~~ and~~

DC offset reduction circuitry coupled to the analog-to-digital converter circuitry,

wherein the DC offset reduction circuitry tends to reduce a DC offset transmitted to the in-phase and quadrature digital output signals; and

a combiner circuitry configured to provide to the analog-to-digital circuitry an in-phase difference signal and a quadrature difference signal,

wherein the combiner circuitry subtracts an in-phase output signal of the DC offset reduction circuitry from the in-phase down-converted signal to produce the in-phase difference signal, and

wherein the combiner circuitry subtracts a quadrature output signal of the DC offset reduction circuitry from the quadrature down-converted signal to produce the quadrature difference signal.

2-3. (Canceled.)

4. (Currently amended) The radio-frequency receiver circuitry of claim ~~3~~1, wherein the DC offset reduction circuitry further comprises a digital-to-analog circuitry configured to provide the in-phase and quadrature output signals of the DC offset reduction circuitry.

5. (Previously presented) The radio-frequency receiver circuitry of claim 4, wherein the DC offset reduction circuitry further comprises a filter circuitry configured to process the in-phase and quadrature digital output signals to provide an in-phase filtered digital output signal and a quadrature filtered digital output signal, the filter circuitry further configured to provide the in-phase and quadrature filtered digital output signals to the digital-to-analog circuitry.

6. (Previously presented) The radio-frequency receiver circuitry of claim 5, wherein a transfer function of the DC offset reduction circuitry has at least one pole the location of which is adjustable over an adjustment cycle of the DC offset reduction circuitry.

7. (Previously presented) The radio-frequency receiver circuitry of claim 6, wherein the location of the at least one pole is adjusted in an initial part of the adjustment cycle of the DC offset reduction circuitry so that the DC offset reduction circuitry tends to settle quickly.

8. (Previously presented) The radio-frequency receiver circuitry of claim 7, wherein the location of the at least one pole is further adjusted in a later part of the adjustment cycle of the DC offset reduction circuitry so that the DC offset reduction circuitry tends to remove the DC offset more accurately.

9. (Previously presented) The radio-frequency receiver circuitry of claim 8, wherein the location of the at least one pole is adjusted by modifying a gain of the DC offset reduction circuitry.

10. (Previously presented) The radio-frequency receiver circuitry of claim 9, wherein the location of the at least one pole is adjusted before a reception of a burst of data begins.

11. (Previously presented) The radio-frequency receiver circuitry of claim 10, wherein the in-phase and quadrature output signals of the DC offset reduction circuitry become substantially constant before the reception of the burst of data begins.

12. (Previously presented) The radio-frequency receiver circuitry of claim 11, wherein the filter circuitry comprises a digital filter circuitry.

13. (Previously presented) The radio-frequency receiver circuitry of claim 12, wherein the digital filter circuitry comprises a low-pass filter circuitry.

14. (Previously presented) The radio-frequency receiver circuitry of claim 13, wherein the low-pass filter circuitry comprises an integrator circuitry.

15. (Previously presented) The radio-frequency receiver circuitry of claim 14, wherein the analog-to-digital converter circuitry comprises a sigma-delta analog-to-digital converter circuitry.

16. (Previously presented) The radio-frequency receiver circuitry of claim 15 used in a radio-frequency transceiver circuitry.

17. (Previously presented) The radio-frequency receiver circuitry of claim 15 used in a low intermediate-frequency (IF) radio-frequency receiver circuitry.

18. (Currently amended) A radio-frequency (RF) receiver circuitry, comprising:

receiver analog circuitry included within a first integrated circuit, the receiver analog circuitry, comprising:

down-converter circuitry configured to receive and down-convert a radio-frequency input signal to generate a down-converted signal;

an analog-to-digital converter circuitry to convert the down-converted signal to a digital output signal; and

DC offset reduction circuitry coupled to the analog-to-digital converter circuitry, wherein the DC offset reduction circuitry tends to reduce a DC offset of the receiver analog circuitry;~~ and~~

receiver digital circuitry included within a second integrated circuit, the receiver digital circuitry configured to receive and process the digital output signal to generate a processed digital signal<u>; and</u>

<u>a combiner circuitry configured to provide a difference signal to the analog-to-digital circuitry, wherein the combiner circuitry subtracts an output signal of the DC offset reduction circuitry from the down-converted signal to produce the difference signal</u>.

19. (Canceled.)

20. (Currently amended) The radio-frequency receiver circuitry of claim ~~19~~<u>18</u>, wherein the DC offset reduction circuitry further comprises a feedback loop that includes a cascade coupling of a filter circuitry and a digital-to-analog circuitry, wherein the filter circuitry receives the digital output signal, and wherein the digital-to-analog circuitry provides the output signal of the DC offset reduction circuitry.

21. (Previously presented) The radio-frequency receiver circuitry of claim 20, wherein a transfer function of the DC offset reduction circuitry has at least one pole the location of which is adjustable so as to modify the settling time of the DC offset reduction circuitry.

22. (Previously presented) The radio-frequency receiver circuitry of claim 21, wherein the location of the at least one pole is adjusted at an initial point in time so that the DC offset reduction circuitry tends to settle quickly.

23. (Previously presented) The radio-frequency receiver circuitry of claim 22, wherein the location of the at least one pole is adjusted at least once more after the initial point in time so that the DC offset reduction circuitry tends to reduce the DC offset more accurately.

24. (Previously presented) The radio-frequency receiver circuitry of claim 23, wherein the location of the at least one pole is adjustable by modifying a gain of the DC offset reduction circuitry.

25. (Previously presented) The radio-frequency receiver circuitry of claim 24, wherein adjustment of the location of the at least one pole completes before a reception of a burst of data by the receiver analog circuitry begins.

26. (Previously presented) The radio-frequency receiver circuitry of claim 25, used within a radio-frequency transceiver circuitry.

27. (Previously presented) The radio-frequency receiver circuitry of claim 25, further comprising programmable gain amplifier circuitry coupled to the combiner circuitry and to the analog-to-digital circuitry, the programmable gain amplifier circuitry configured to apply a programmable gain to the difference signal to produce an amplified difference signal, the programmable gain amplifier circuitry further configured to provide the amplified difference signal to the analog-to-digital converter circuitry.

28. (Previously presented) The radio-frequency receiver circuitry of claim 27, used within a radio-frequency transceiver circuitry.

29. (Currently amended) A method of receiving a radio-frequency (RF) signal, comprising:

down-converting the radio-frequency signal within a receiver analog circuitry to generate a down-converted signal;

converting the down-converted signal to a digital output signal by using an analog-to-digital converter circuitry that resides within the receiver analog circuitry; and

feeding back to an input of the analog-to-digital converter circuitry a feedback signal that relates to the digital output signal<u>, by subtracting the feedback signal from the down-converted signal to generate a difference signal and supplying the difference signal to the input of the analog-to-digital converter circuitry,</u>

wherein feeding back the feedback signal to an input of the analog-to-digital converter tends to reduce a DC offset of the receiver analog circuitry.

30. (Canceled.)

31. (Currently amended) The method of claim ~~30~~29, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises:

filtering the digital output signal to generate a filtered digital signal; and

converting the filtered digital signal to the feedback signal by using a digital-to-analog converter circuitry.

32. (Previously presented) The method of claim 31, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry comprises adjusting a location of at least one pole within the receiver analog circuitry.

33. (Previously presented) The method of claim 32, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises adjusting at an initial point in time the location of the at least one pole so that the DC offset tends to be reduced quickly.

34. (Previously presented) The method of claim 33, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises adjusting the location of the at least one pole at least once more after the initial point in time so that the DC offset tends to be reduced accurately.

35. (Previously presented) The method of claim 34, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises adjusting the location of the at least one pole by modifying a gain within the receiver analog circuitry.

36. (Previously presented) The method of claim 35, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises completing the adjustment of

the location of the at least one pole before a reception of a burst of data by the receiver analog circuitry begins.

37. (Previously presented) The method of claim 36, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises holding substantially constant the feedback signal before a reception of a burst of data begins.

38. (Previously presented) The method of claim 37, wherein feeding back the feedback signal to the input of the analog-to-digital converter circuitry further comprises:

applying a programmable gain to the difference signal to produce an amplified difference signal; and

supplying the amplified difference signal to the input of the analog-to-digital converter circuitry.

39. (Previously presented) The method of claim 38, wherein converting the down-converted signal to a digital output signal comprises using a sigma-delta analog-to-digital converter circuitry that resides within the receiver analog circuitry.

40. (Previously presented) The method of claim 39, further comprising supplying the digital output signal to a receiver digital circuitry.

41. (Previously presented) The method of claim 40, further comprising processing the digital output signal in the receiver digital circuitry to generate a baseband signal.

42. (Previously presented) The method of claim 41, further comprising providing the baseband signal to a baseband processor circuitry.

43. (Previously presented) The method of claim 42, wherein receiving the radio-frequency signal further comprises receiving the radio-frequency signal within a low intermediate-frequency radio-frequency receiver circuitry.

44. (Previously presented) The method of claim 43, wherein receiving the radio-frequency signal further comprises receiving the radio-frequency signal within a radio-frequency transceiver circuitry.